

# FDP7N50U/FDPF7N50U

## 500V N-Channel MOSFET

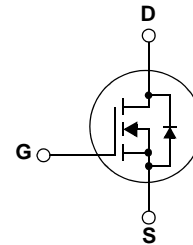
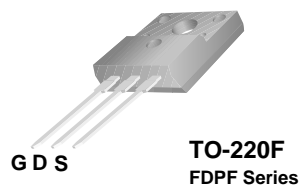
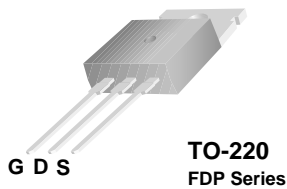
### Features

- 5A, 500V,  $R_{DS(on)} = 1.5\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 12.8 nC)
- Low  $C_{rss}$  ( typical 9 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



### Absolute Maximum Ratings

Symbol	Parameter	FDP7N50U	FDPF7N50U	Unit
$V_{DSS}$	Drain-Source Voltage	500		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	5	5 *	A
		3.0	3.0 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	20	20 *	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	270		mJ
$I_{AR}$	Avalanche Current (Note 1)	5		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.9		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	89	39	W
		0.71	0.31	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FDP7N50U	FDPF7N50U	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.4	3.2	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP7N50U	FDP7N50U	TO-220	--	--	50
FDPF7N50U	FDPF7N50U	TO-220F	--	--	50

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

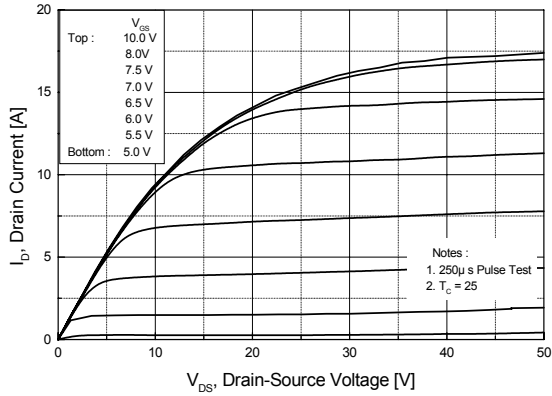
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 400V, T <sub>C</sub> = 125°C	--	--	25 250	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A	--	1.2	1.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 2.5A (Note 4)	--	2.5	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	720	940	pF
C <sub>oss</sub>	Output Capacitance		--	95	190	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	9	13.5	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 7A R <sub>G</sub> = 25Ω  (Note 4, 5)	--	6	20	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	25	60	ns
t <sub>f</sub>	Turn-Off Fall Time		--	35	80	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400V, I <sub>D</sub> = 7A V <sub>GS</sub> = 10V  (Note 4, 5)	--	12.8	16.6	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.7	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	5.8	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	5	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	20	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A	--	--	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A di <sub>F</sub> /dt = 100A/μs  (Note 4)	--	40	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.04	--	μC

### NOTES:

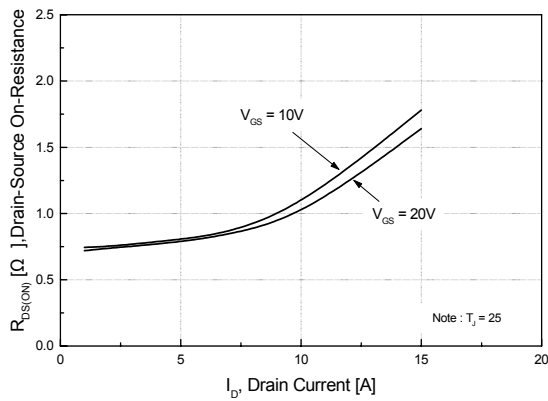
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 7A, V<sub>DD</sub> = 50V, L = 10mH, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 7A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

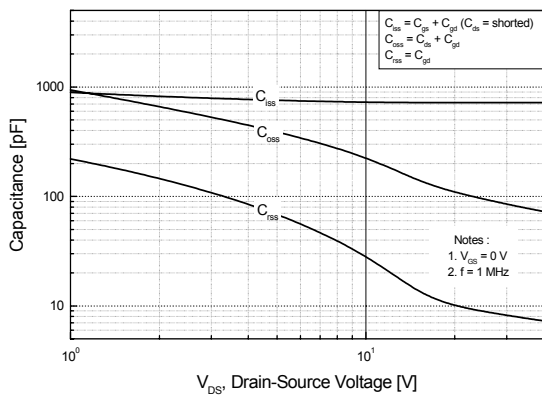
**Figure 1. On-Region Characteristics**



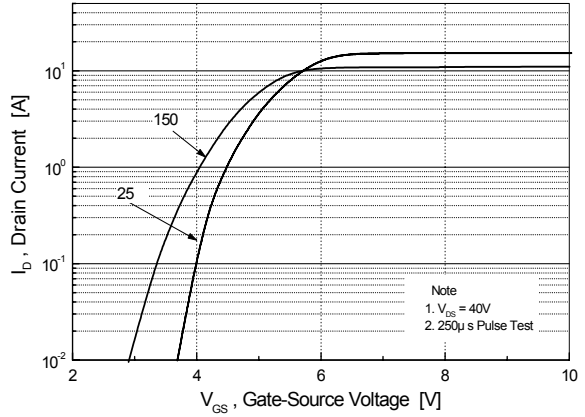
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



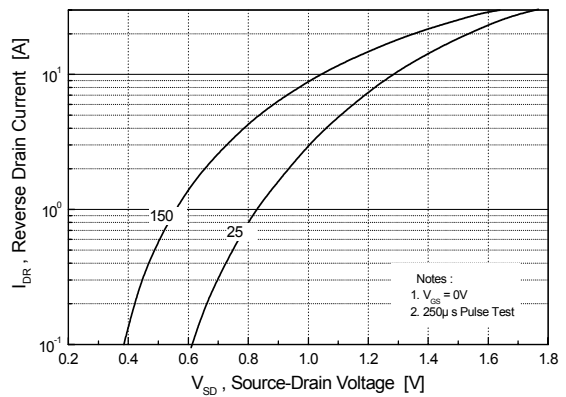
**Figure 5. Capacitance Characteristics**



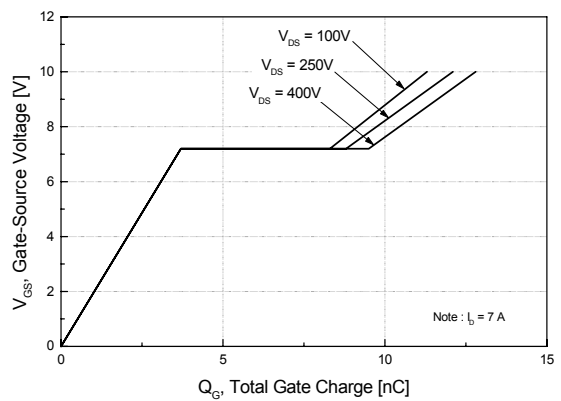
**Figure 2. Transfer Characteristics**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

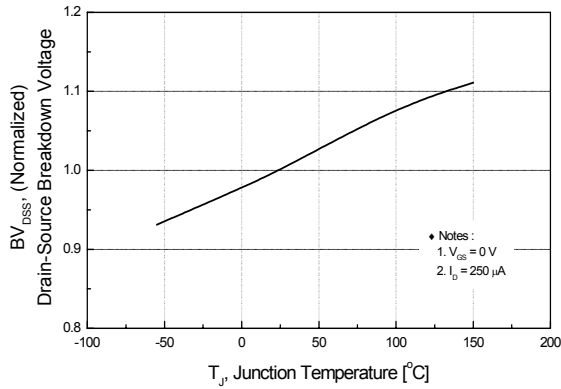


**Figure 6. Gate Charge Characteristics**

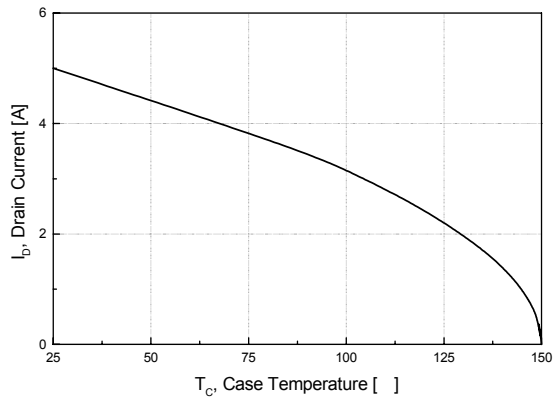


**Typical Performance Characteristics (Continued)**

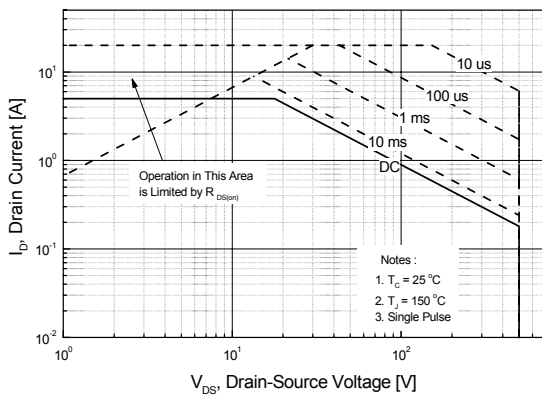
**Figure 7. Breakdown Voltage Variation vs. Temperature**



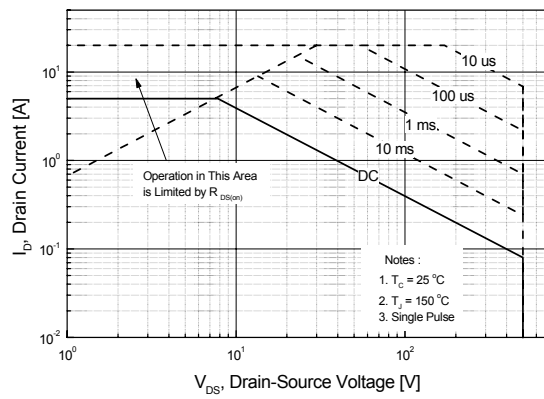
**Figure 8. Maximum Drain Current Vs. Case Temperature**



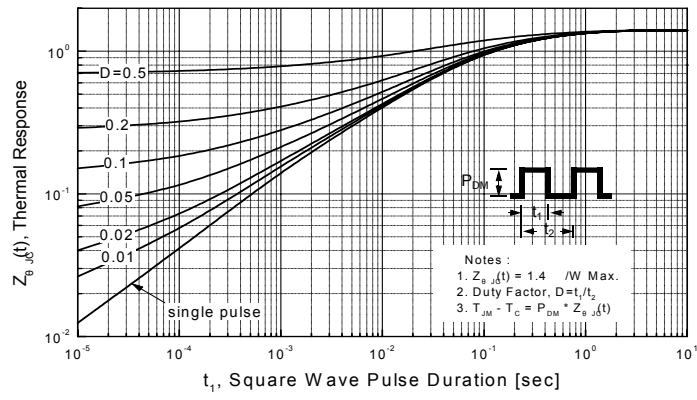
**Figure 9-1. Maximum Safe Operating Area - FDP7N50U**



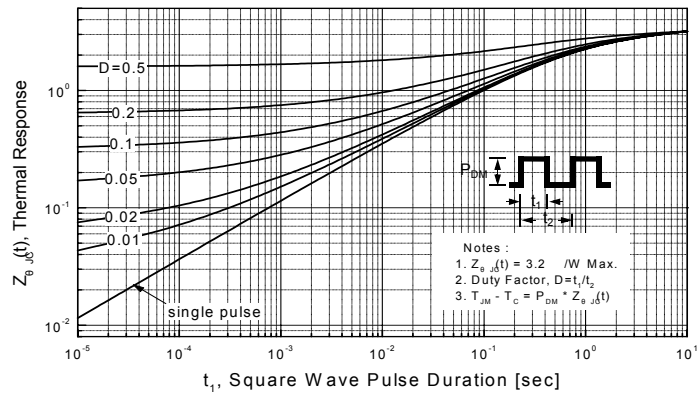
**Figure 9-2. Maximum Safe Operating Area - FDPF7N50U**



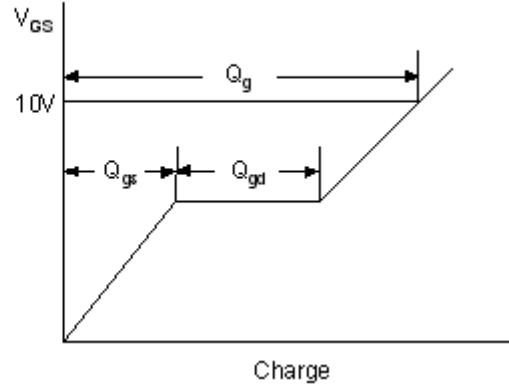
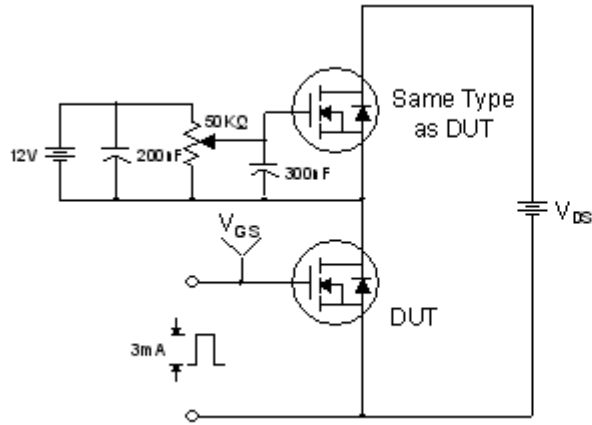
**Figure 10-1. Transient Thermal Response Curve - FDP7N50U**



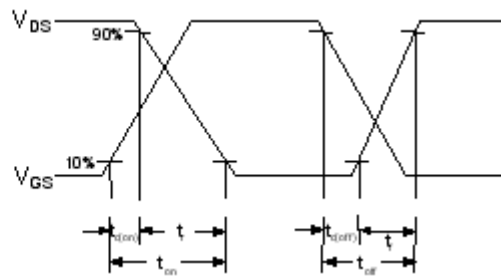
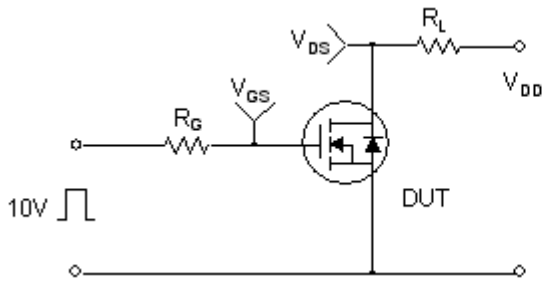
**Figure 10-2. Transient Thermal Response Curve - FDPF7N50U**



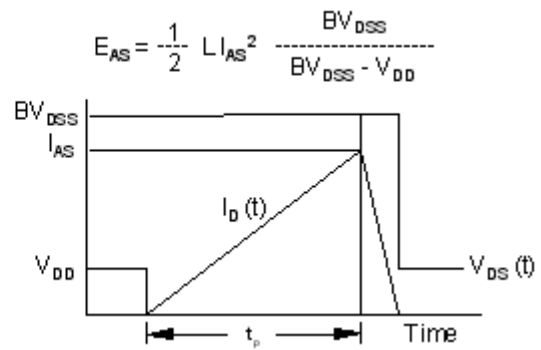
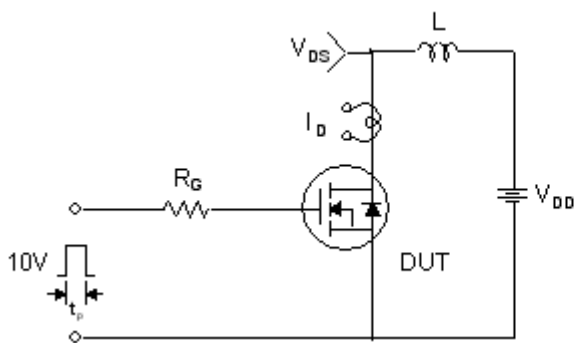
**Gate Charge Test Circuit & Waveform**



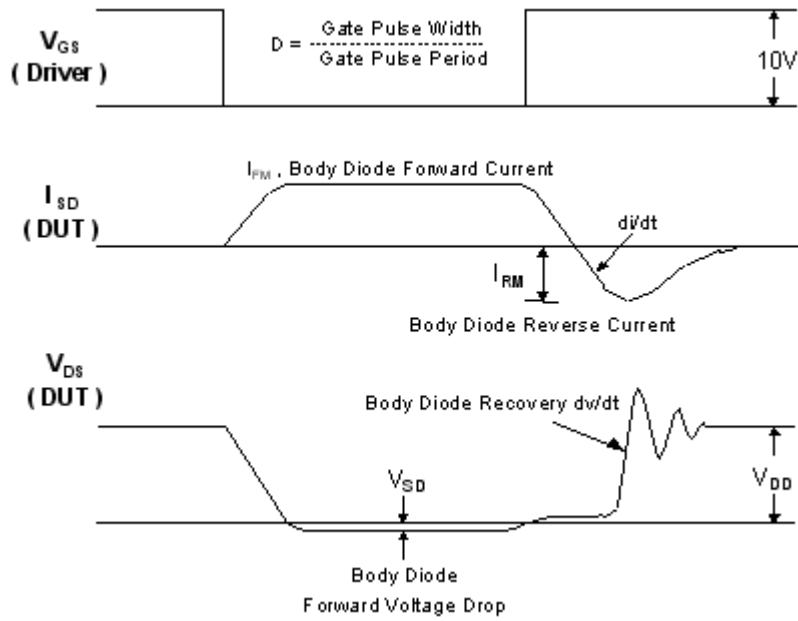
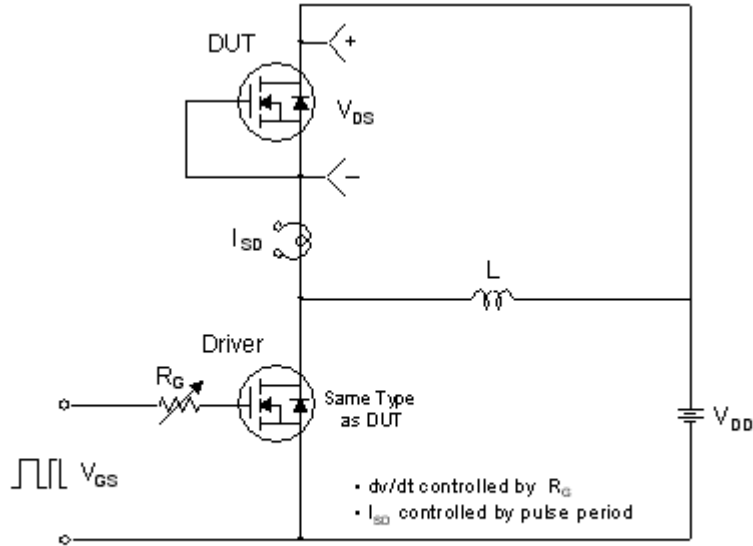
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

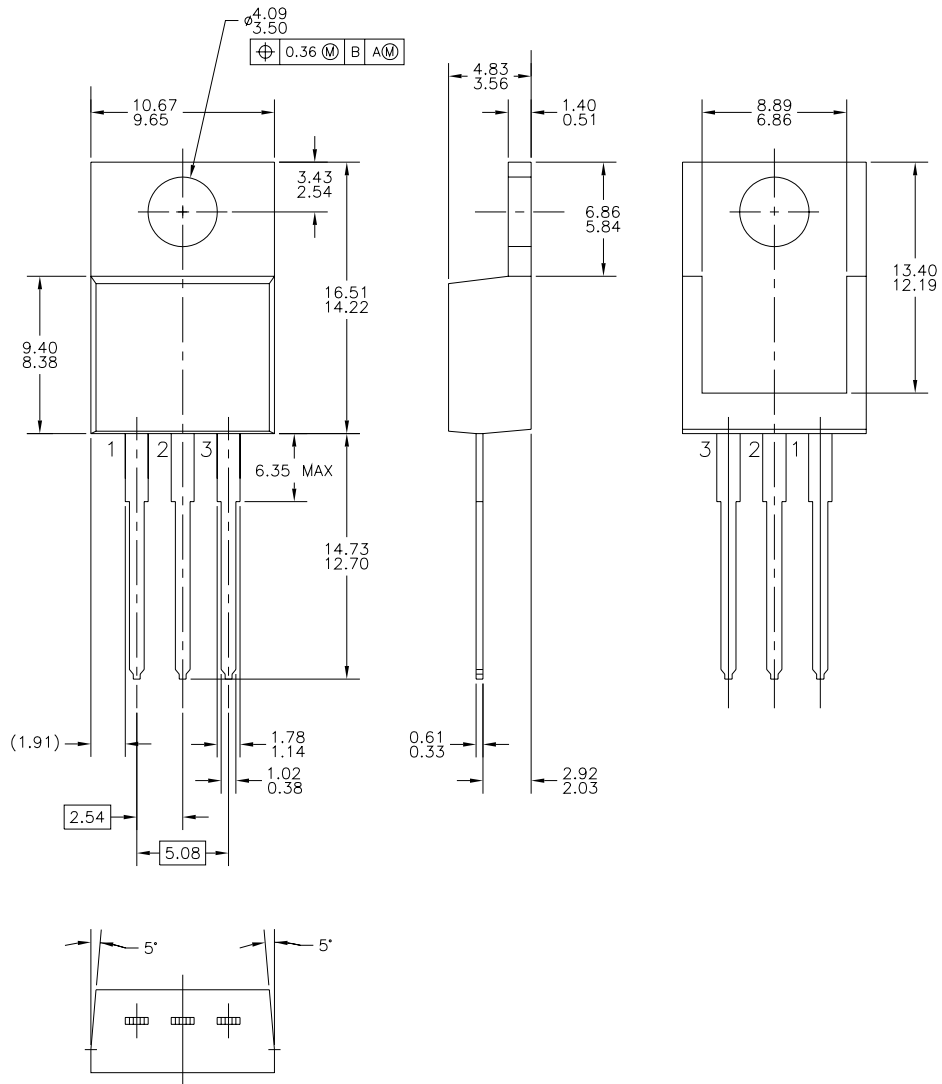


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220

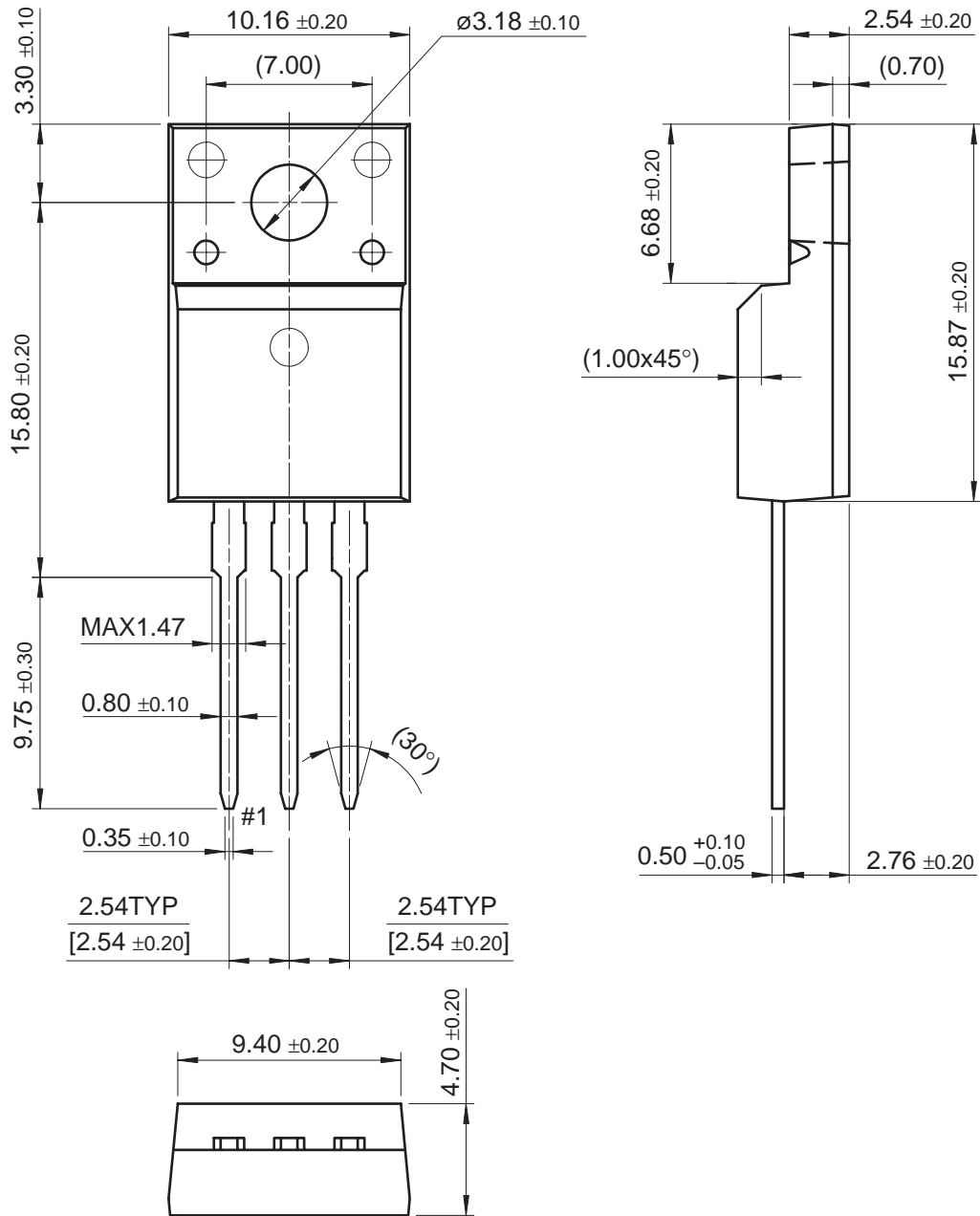


Dimensions in Millimeters



Mechanical Dimensions (Continued)

TO-220F




Dimensions in Millimeters



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